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DESIGN AND SYNTHESIS FOR DEEP LEARNING AND MULTILAYER NEURAL NETWORK ARCHITECTURE USING VHDL

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ABSTRACT

Artificial neural networks are extended on the basis of brain structure. Like the brain, ANNs can recognize patterns, handle facts and figures and be trained. They are prepared by artificial neurons which employ the quintessence of genetic neurons. In the research work, we have considered the 8 inputs ANN signal which is multiplied with their corresponding weights. The hardware chip is designed to support the system functionality in Xilinx ISE 14.2 software. The designed chip is simulated with Modelsim 10.0 software for test cases. The designed chip is also synthesized on SPARTAN-3E FPGA using VHDL programming and device hardware and timing parameters are also analyzed for the functionality of the chip.

KEYWORDS: Artificial Neural Network (ANN), FPGA, Xilinx ISE software.

1. INTRODUCTION

An ANN [1, 2] is based on a gathering of connected units or nodes called artificial neurons which loosely model the neurons in a biological brain. Each connection, like the synapses in a biological brain, can transmit a signal from one artificial neuron to another. An artificial neuron [3, 4] that receives a signal can process it and then signal supplementary artificial neurons connected to it. In general ANN implementations, the signal at a connection between artificial neurons are a real number, and the output of each artificial neuron is computed by some non-linear function of the sum of its inputs. The connections between artificial neurons are called 'edges'. Artificial neurons and edges typically have weights [5, 6] that adjust as knowledge proceeds. The weight increases or decreases the strength of the signal at a connection. Artificial neurons [3, 7] may have a threshold such that the signal is only sent if the aggregate signal crosses that threshold. Typically, artificial neurons are aggregated into layers. Different layers may perform different kinds of transformations on their inputs. Signals travel from the first layer (the input layer) to the last layer (the output layer), possibly after traversing the layers multiple times. The main objective of the ANN-based approach is to solve the real problems as the human brain is cable to solve. However, the computations will involve the functioning of specific tasks, leading to the deviations from biology. The artificial neural networks are applied for the different variability of tasks, including machine learning [10], computer vision, social networks, video games, network filtering, computer vision, speed recognition, machine translation, speech recognition, filtering, social network and medical applications.

ANN architecture

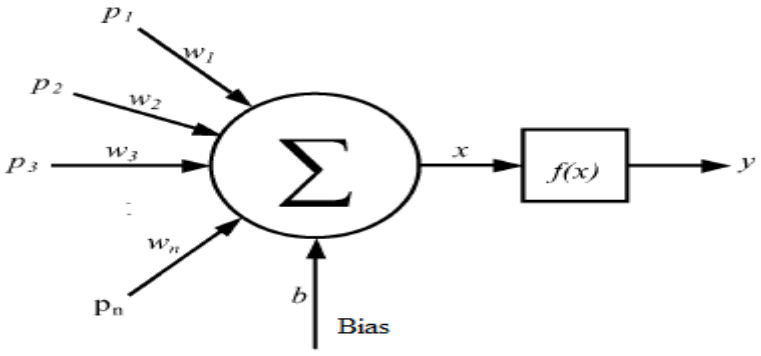

Fig. 1: Neuron structure

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The general model of the neural network is shown in fig. 1.3. It has the 'n' number of inputs. Let us consider that the inputs are p_1, p_2, p_3……p_n. These inputs are processed with their corresponding weights as w_1, w_2, w_3…...w_n and 'b' is the bias input. The nonlinear execution function [21, 22] is f(x). The neuron processing is expressed with the help of equation.

The w_i is referred as the weights for the i^{th} connections and b is the bias inputs. The behavior of the function f(x) is nonlinear excitation function. The most popular excitation function used are expressed as
For linear function,

$$f(x) = x$$

For log sigmoid function,

$$f(x) = \frac{1}{1 + e^{-x}}$$

For tan sigmoid function,

$$f(x) = \frac{e^{x} - e^{-x}}{e^{x} + e^{-x}}$$

2. RESULTS AND DISCUSSIONS

The Xilinx software simulation results for 8 input ANN Architecture is shown in figure 2 that presents the RTL level view of the developed chip. The RTL provides the details of all the pins used for the design of the chip. The Modelsim simulation result is shown in figure 3 that presents the simulation output of two test cases.

Test-1 :

P1<7:0> = "00000011" in binary = 3 in decimal, P2<7:0> = "00000100" in binary = 4 in decimal, P3<7:0> = "00000101" in binary = 5 in decimal, P4<7:0> = "00000110" = 6 in decimal, P5<7:0> = 00000101" in binary = 5 in decimal, P6<7:0> ="00000100" in binary = 4 in decimal, P7<7:0> = "00000011" in binary = 3 in decimal, P8<7:0> = "00000010" in binary = 2 in decimal, W1<7:0> = "00000001" in binary = 1 in decimal, W2<7:0> = "00000010" in binary = 2 in decimal W3<7:0> ="00000011" in binary = 2 in decimal, W4<7:0> ="00000010" in binary = 2 in decimal, W5<7:0> = "00000010" = 2 in decimal, W6<7:0> = "00000001" = 1 in decimal, W7<7:0> = "00000001" = 1 in decimal, W8<7:0> = "00000010" = 2 in decimal, b_i<15:0> = "0000000110111100" = 220 in decimal, Then output will be Y <15:0> = "0000000100010111" = 279 in decimal.

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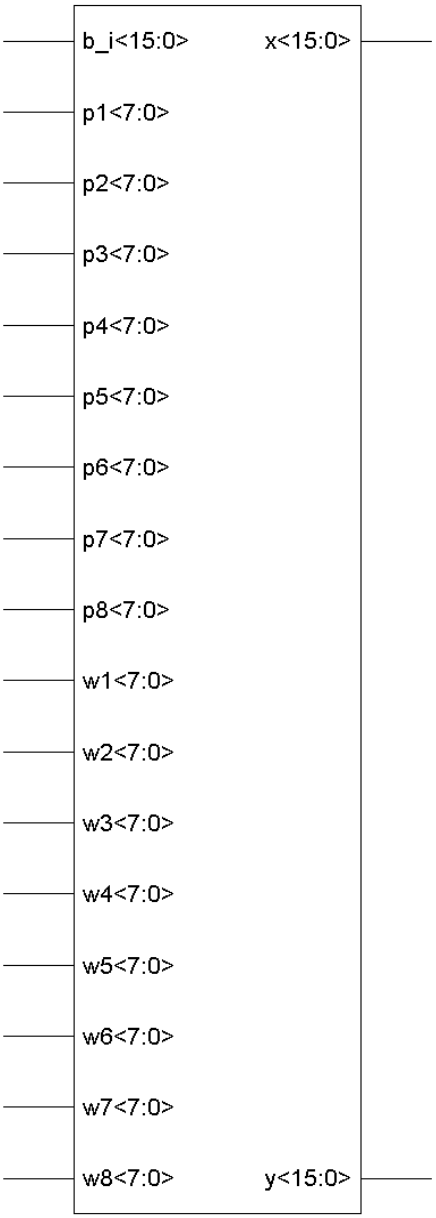

Fig. 2: RTL View of 16-Point ANN architecture chip

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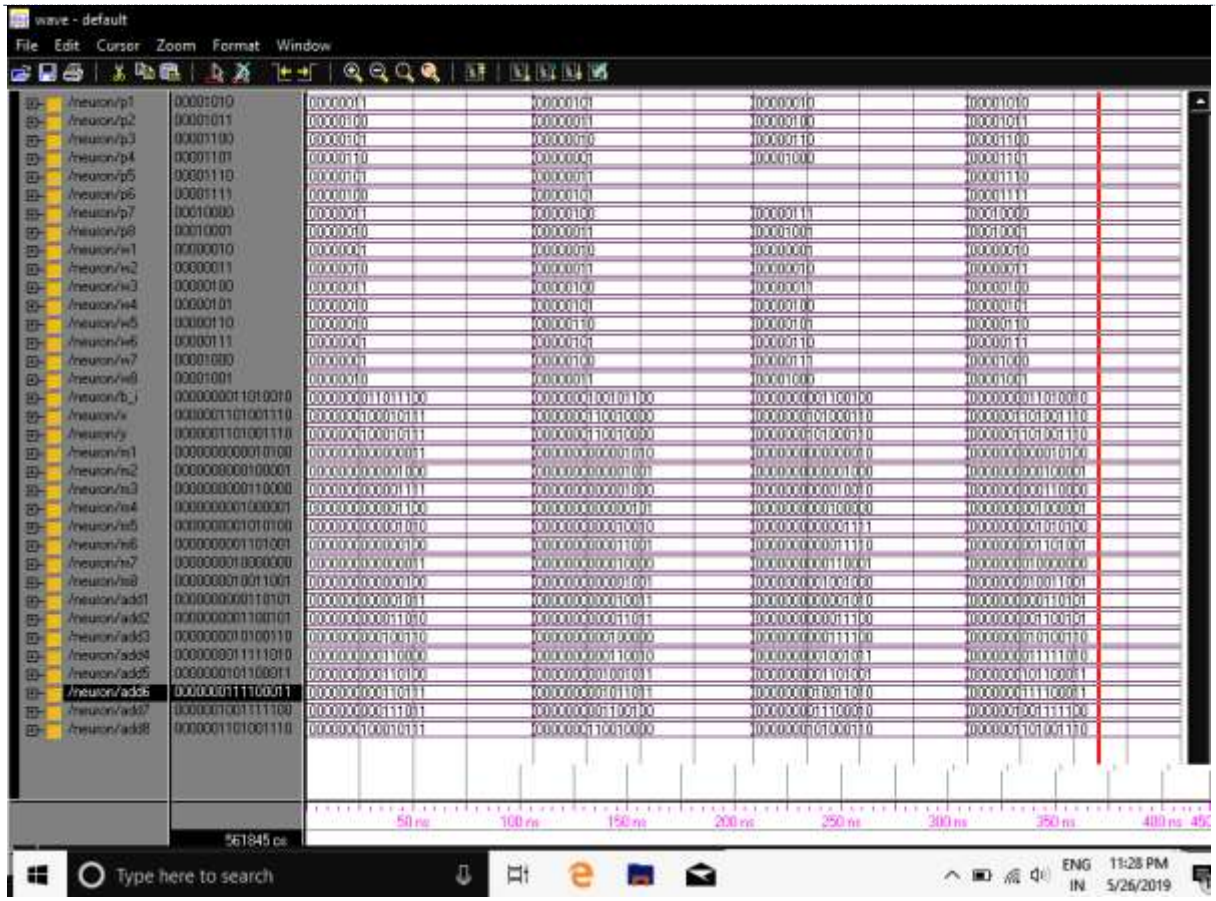

Fig.3 Modelsim simulation of 8 input ANN with test-1

3. XILINX DEVICE UTILIZATION SUMMARY

Xilinx is one of the largest manufacturers of FPGA and ASIC based solutions. Xilinx has become the semiconductor industry leader in business targets, market coverage of the forefront of technology. In the Xilinx, the designer can develop the code using any HDL programming language such as VHDL or Verilog HDL. After that, the design is checked and functionality simulated in the Xilinx. In this tool, the chip is designed to design and its Register Transfer Logic (RTL) view and schematic can be seen. It is a tool used to test the code on the FPGA platform with different test benches. The tool provides complete information of simulation, synthesis, and timing analysis. The pre-synthesis parameters can be extracted from the tool such as hardware parameters, timing parameters and memory utilization etc. The percentage of hardware that is used by the device is given by the device utilization report for the implementation of chip. Device hardware includes No. of slices. Of input LUTs, No. of bounded IOBs and No. of Gated Clocks (GCLKs) used in design implementation. Timing details provides the knowledge of the maximum frequency and combinational delay. To complete the design, the total memory utilization required is also given. The Xilinx software gives the details of the hardware utilization for 8 input ANN. Table 1 presents the utilization report of the hardware parameters and table 2 presents the timing results.

Test-2:

P1 = “00000101” in binary = 5 in decimal, P2“00000011” in binary = 3 in decimal, P3 = “00000010” in binary = 2 in decimal, P4 = “00000001” = 1 in decimal, P5 = “00000011” in binary = 3 in decimal, P6 = 00000101” in binary = 5 in decimal, P7 = “00000100” in binary = 4 in decimal, , P8 = “00000011” in binary = 3 in decimal , W1 = “00000010” in binary = 2 in decimal, W2 = “00000011” in binary = 3 in decimal W3 = “00000100” in binary = 4 in decimal, W4 =“00000101” in binary = 5 in decimal, W5 = “00000110” = 6 in decimal, W6 = “00000101” in binary = 5 in decimal, W7 = “00000100” in 45 binary = 4 in decimal, W8 = “00000011” = 3 in

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decimal, b_i = "0000000100101100" = 300 in decimal, Then output will be Y = "0000001100100000" =400 in decimal.

Table 1: Hardware summary for 16 input ANN for SPARTAN 3E FPGA

Parameter	**ANN (8 input)**	**ANN (16 input)**	**ANN (32 input)**	**ANN (64 input)**
Slices Usage	355	710	1420	2807
Slice flipflops	418	524	1014	1608
LUTs Usage	648	1025	2212	5120
IoBs	178	181	181	181
GCLKs	1	1	1	1
Memory Usage	116688 kB	121518 kB	142791 kB	166868 kB

4. CONCLUSION

A neural network is produced by a sequence of nodes called neurons that are structured in layers. Each neuron in a layer is associated with each neuron in the next layer through a weighted relationship. The hardware chip of 16 input ANN architecture is designed in Xilinx ISE 14.2 software successfully and simulated in Modalism 10.0 software. The designed chip is synthesized on SPARTAN-3E FPGA. The designed chip support the frequency of 235 MHz. The timing detail parameters are a minimum period (ns), the minimum time before clock signal (ns), maximum time after clock signal (ns) and combinational delay (ns) which are estimated as 2.417 ns, 3.240 ns, 6.290 ns and 9.120 ns respectively.

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